

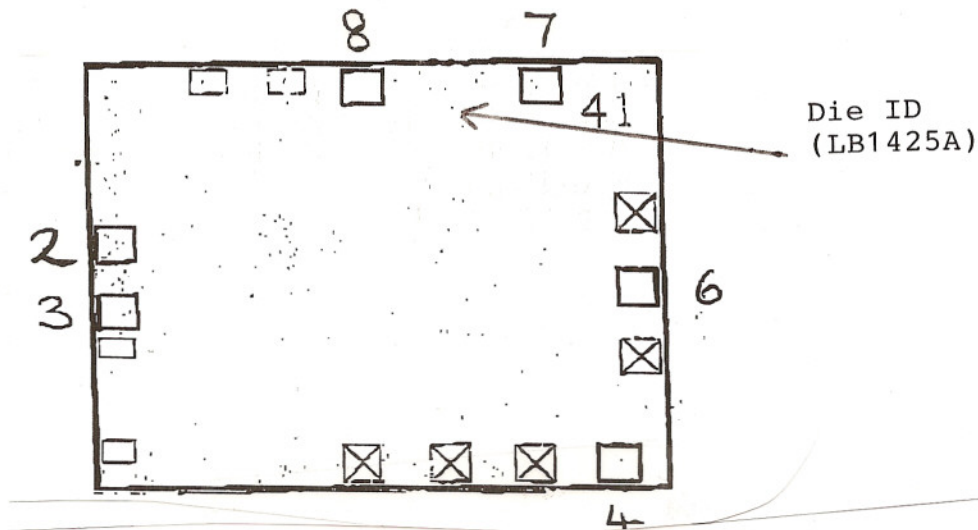


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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Pad Function

1	NC
2	V_{inv}
3	$V_{non-inv}$
4	$-V_{CC}$
5	NC
6	V_{out}
7	$+V_{CC}$
8	DIS

Topside Metal: Au

Backside: Au

Backside Potential: -vCC

Mask Ref: 41

Bond Pads (Mils): 4 X 4

APPROVED BY:

MFG: National

DIE SIZE (Mils): 66 X 56

THICKNESS: 14

DATE: 3/16/00

P/N: CLC430